Training Opportunity for Portuguese Trainees

**Reference**
PT-2013-TEC-EDM(2)

**Title**
Hyper Spectral Image Compression IP development

**Duty Station**
ESTEC

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### Overview of the Unit missions:

The unit of destination of the trainee is TEC-EDM, microelectronics section. The section is in charge of providing ASIC and FPGA technical support to ESA projects and of undertaking and coordinating R&D activities for new microelectronic technologies, including EDA tools, IP Cores, design methodology, HW-SW co-design, ASIC digital and analogue libraries.

The initiating entity TEC-EDM (micro-electronics section) will cooperate with other sections such as TEC-EDP (payloads section) responsible for image compression algorithm definition and TEC-SWE (software section) responsible for embedded software and operating systems.

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### Overview of the field of activity proposed:

This activity aims at developing a new SystemC/VHDL IP implementing an algorithm for hyper spectral image compression. This algorithm will most likely be the basis for future CCSDS standardisation. Nevertheless while still subject to potential evolutions, making an hardware implementation (FPGA prototype) will also help to better drive the future standard. The following tasks will be performed in the frame of this activity:

- Algorithm Literature review
- Algorithm compilation (C/C++ golden reference model)
- C/C++ test benches compilation and execution

For the first 3 tasks, documentation and golden reference models (C/C++) already exist. The candidate will have to understand the algorithm and install the “golden reference” simulation framework. Then from this point the candidate will have to perform the following tasks:

- Learn SystemC language and “Transactional Level Modelling” (TLM)
- Learn High Level Synthesis concepts based on Cadence tool “C2Silicon”
- Write a SystemC TLM model suitable with Cadence high level synthesis tool “C2Silicon”
- Write high level synthesis scripts
- Perform algorithm architecture exploration
- Generate VHDL RTL code using “C2Silicon” compiler
- Write logic synthesis scripts
- Run logic synthesis + static timing analysis + place&route tools targeting FPGA implementation Xilinx Virtex6 and/or Microsemi ProASIC 3/4 technologies
- Implement the algorithm on a FPGA board
- Validate the algorithm in a lab environment
- Generate documentation related to the new IP
- Generate IP data pack including documentation + source code + test benches + synthesis scripts + synthesis reports targeting various FPGA and/or ASIC technologies

Assuming the tasks listed here above would be completed successfully the candidate would then be proposed additional (optional) work focussing on hardware/software co-design and SoC virtual platform development.

- Profile the SystemC model and identify the compute intense parts of the code requiring hardware acceleration
- Profile the SystemC model and identify the parts requiring more flexibility and software programmability
- Propose a hardware-software partitioning
- Develop a SystemC TLM virtual platform including the following hardware IPs:
- Hardware acceleration unit supporting hyper spectral image compression
- LEON3 core (Sparc V8 architecture) and/or TI DSP (TMS 320 C 6748)
- SpaceWire interfaces

- Compile the application software on the virtual platform
- Simulate the virtual platform and associated compiled software
- Validate algorithm performances and hardware-software partitioning assumptions
- If assumptions verified then generate VHDL RTL code if assumptions not verified then propose a new partitioning
- Run logic synthesis + static timing analysis + place&route tools targeting FPGA implementation Xilinx Virtex6 and/or Microsemi ProASIC 3/4 technologies
- Implement the algorithm on a FPGA board
- Validate the algorithm in a lab environment

Hyper spectral image compression background:

The Lossy Compression for Exomars (LCE) algorithm was developed in Politecnico di Milano and was designed to achieve high coding efficiency while meeting other very important requirements for on-board compression at the same time, namely low complexity, error-resilience and hardware friendliness. Low complexity is achieved by applying a simple predictor plus a Golomb power-of-two entropy coder instead of arithmetic coding. In order to make it error resilient, the data is partitioned into units which are coded independently, in such a way that an error in one unit will not affect the decoding of other units. The LCE algorithm was also designed so that its hardware implementation is simple and easy to parallelize in order to speed up the process for high data-rate sensors. The algorithm has been submitted to the CCSDS Data Compression Working Group for possible standardization.

Ref.: A. Abrardo, M. Barni, E. Magli. “Low-complexity predictive lossy compression of hyperspectral and ultraspectral images”, in Acoust., Speech and Signal Processing. (ICASSP), 2011 IEEE Int. Conf. on, may 2011, pp. 797-800

Required Education:

Applicants should have just completed, or be in their final year of a University course at Masters level in Electrical or Computer Engineering. A strong background in Software Engineering and C/C++ programming is required and knowledge of Hardware Description Languages (mainly VHDL) is welcome. Candidates must be fluent in English and/or French, the official languages of the Agency. Candidates should have a high degree of autonomy together with an attitude to work in an international team environment. They should have good communication skills and an interest into innovative technologies.