

## Training Opportunity for Portuguese Trainees

Reference	Specialist Area	Duty Station
PT-2012-TEC-EDM	MICROELECTRONICS	ESTEC
<p><b><u>Overview of the Division missions:</u></b></p> <p>ASIC and FPGA technical support to ESA projects. R&amp;D for new microelectronics technologies (EDA tools, IPs, design methodology, HW-SW co-design, ASIC digital and analogue libraries, etc).</p>		
<p><b><u>Overview of the field of activity proposed:</u></b></p> <p>Summary of <b>MICROELECTRONICS TOPICS</b> for trainee work, to be defined and tailored to specific trainee background and interests:</p> <ol style="list-style-type: none"> <li>1. HW/SW validation tests of already developed System-on-Chip designs for spacecraft control. We already have several SoCs on FPGA on validation boards. The work would be about gathering additional test equipment, and conducting validation tests which would involve generation and use of LEON uP drivers, and exercising the various data/control internal and external interfaces. More details on several SoC ASICs (NGMP-Quad LEON4, SCOC3, SpW-RTC, SpW-10X Router, etc) are here: <a href="http://www.esa.int/TEC/Microelectronics/SEMT4VU681F_0.html">http://www.esa.int/TEC/Microelectronics/SEMT4VU681F_0.html</a></li> <li>2. Perform HW/SW validation tests on diverse "SystemC &amp; VHDL IP Cores" that have been recently developed and will be maintained and offered to the Space Industry by ESA. There are several options SpaceWire-D, CANopen, etc: <a href="http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html">http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html</a></li> <li>3. In house validation and debugging of new reprogrammable FPGA for space applications (ATMEL AT280K, 450K, Raptor, Actel ProASIC)</li> <li>4. Research on advanced SoC design methodology which involve System-C modeling and simulation, SystemC+VHDL+C co-simulation, high use of building blocks (IP) re-use and automatic generation and integration, analysis of the potential of emerging on-chip communication protocols (OCP-IP, Network-on-Chip) and multiprocessor architectures.</li> <li>5. Analogue design for radiation hardened ASIC digital and analog library cells. Porting of Rad Hard libraries from one process to another, with help of porting tools (e.g. ANACONDA).</li> <li>6. Study and the implementation of an efficient placing (and possibly routing)</li> </ol>		

algorithm for SRAM-based ATMEL FPGAs, with the aim of overcoming the current limitations of the present ATMEL tool. Following up on a previous Microelectronics trainee, the work will consist in improving the algorithm to take into account, in addition to performance, reliability and hardening against faults of the circuit, done in four phases: (1) Study of the ATMEL FPGA architecture and of the state of the art in terms of placing and routing algorithms; (2) acquisition of background knowledge on the current tools used to program ATMEL FPGAs and the existing research results so far. (3) Implementation of placement and/or routing algorithms, trying to overcome the deficiencies of the current ATMEL ones. (4) Testing of the implemented solutions on different circuits and FPGA model to assess the robustness of the devised mechanisms.

7. Microcontrollers for space applications: review of existing free, soft-core micro-controllers, analysis of potential modifications to improve reliability in space applications, develop a software layer (Board SW Package). Also development of analogue IP blocks that could be integrated in a future space microcontroller.
8. R&D on SystemC-Analogue Mixed Signal methodology and tools, including multiple elements: (1) Establishing the tool flow for systemc-ams simulations. (2) Systemc-ams modelling of key analogue and mixed signal components: Ina,pa,filter, adc/dac, sampler leading eventually to the modelling of the physical layer of a wired and wireless communication interface. This could be spi, i2c, spw, can, mil-bus-1553 or 802.15.14 (Zigbee) (3) Comparison of system simulation performance of systemc and vhdl-ams and spice. (4) Simulation of a module, like a power distribution and management system or a payload processor or instrumentation front-end, that verifies its behaviour under redundancy, for single point failures and for different operational configurations and scenarios.

### **Required Education:**

For MICROELECTRONICS: Applicants should have just completed, or be in their final year of a University course at Masters level in Electrical Engineering (other degrees such as Industrial Engineering, Computer Engineering or Physics could be suitable, as long as the trainee has a solid Electronics background, preferably in Microelectronics, and also including experience with digital or analogue IC design, CAD and test tools, and relevant IC design languages).

Candidates must be fluent in English and/or French, the official languages of the Agency. Candidates should have a high degree of autonomy together with an attitude to work in an international team environment. They should have good communication skills and an interest in innovative technologies.